L Number	Hits	Search Text	DB	Time stamp
4	6387	(barrier with (first or second)) and conductive and substrate	USPAT; US-PGPUB	2002/05/31 16:51
5	3548	((barrier with (first or second)) and conductive and substrate) and dielectric	USPAT; US-PGPUB	2002/05/31 16:51
7	3057	(((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)	USPAT; US-PGPUB	2002/05/31 16:52
8	927	((((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)) and (barrier same (silicon adj nitride)or (silicon adj carbide))	USPAT; US-PGPUB	2002/05/31 16:52
9	923	(((((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)) and (barrier same (silicon adj nitride)or (silicon adj carbide))) and @ad<=20020102	USPAT; US-PGPUB	2002/05/31 14:52
10	875	((((((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)) and (barrier same (silicon adj nitride)or (silicon adj carbide))) and @ad<=20020102) and etch$3	USPAT; US-PGPUB	2002/05/31 14:53
11	829	((((((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)) and (barrier same (silicon adj nitride)or (silicon adj carbide))) and @ad<=20020102) and (first with second)	USPAT; US-PGPUB	2002/05/31 14:54
13	0	((((((((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)) and (barrier same (silicon adj nitride)or (silicon adj carbide))) and @ad<=20020102) and (first with second)) and ((via or trench or opening or hole) with (polymer or spin))) and (dyed with (polymer or glass))	USPAT; US-PGPUB	2002/05/31 14:56
12	68	(((((((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)) and (barrier same (silicon adj nitride)or (silicon adj carbide))) and @ad<=20020102) and (first with second)) and ((via or trench or opening or hole) with (polymer or spin))	USPAT; US-PGPUB	2002/05/31 16:06
14	1	("5543644").PN.	USPAT; US-PGPUB	2002/05/31 16:01
15	645	(barrier with (first or second)) and conductive and substrate	EPO; JPO; DERWENT; IBM_TDB	2002/05/31 16:51
16	202	((barrier with (first or second)) and conductive and substrate) and dielectric	EPO; JPO; DERWENT; IBM_TDB	2002/05/31 16:52
17	108	(((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)	EPO; JPO; DERWENT; IBM_TDB	2002/05/31 16:52
18	9	((((barrier with (first or second)) and conductive and substrate) and dielectric) and (via or trench or opening or hole)) and (barrier same (silicon adj nitride)or (silicon adj carbide))	EPO; JPO; DERWENT; IBM_TDB	2002/05/31 16:52

PGPUB-DOCUMENT-NUMBER: 20020001941
DOCUMENT-IDENTIFIER: US 20020001941 A1
TITLE: SEMICONDUCTOR DEVICE MANUFACTURING METHOD

---------- KWIC ---------

ABTX:
The dual damascene method having steps of; after a **first** insulating film, a **first** organic insulating film, a **second** insulating film, and a metal film are formed in sequence, a **first opening** having a wiring pattern is formed in the metal film, then a **second opening having a via** pattern is formed in the **second** insulating film, then the **first** organic insulating film is etched using the **second** insulating film as a mask, then the **first** insulating film and the **second** insulating film are etched simultaneously while using the metal film and the **first** organic insulating film as a mask, and then the **first** organic insulating film is etched while using the metal film as a mask, at this stage, a wiring recess is formed in the **first** organic insulating film and the **second** insulating film, and a via-hole is formed in the **first** insulating film.

BSTX:
[0014] **First,** as shown in FIG. 1A, a **first** silicon oxide film 2, an organic low dielectric constant film 3, and a **second** silicon oxide film 4 are formed in sequence on a silicon substrate 1. In this case, fluorocarbon polymer such as polytetrafluoroethylene is employed as material of the organic low dielectric constant film. Then, an opening 4a having a wiring profile is formed in the second silicon oxide film 4 by patterning the second silicon oxide film 4.

Then, as shown in FIG. 1B, resist is formed on the second silicon oxide film 4 and the opening 4a. A plug window 5a is formed on a part of the opening 4a by exposing/developing the resist. The resultant resist is employed as a resist pattern 5. Then, as shown in FIG. 1C, a via-hole 6 is formed by etching the organic low dielectric constant film 3 and the first silicon oxide film 2 in sequence through the plug window 5a of the resist pattern 5. Then, as shown in FIG. 1D, a wiring recess 7 is formed by selectively etching the organic low dielectric constant film 3 by the oxygen plasma through the opening 4a of the second silicon oxide film 4. Then, although not particularly shown, copper is buried in the via-hole 6 and the wiring recess 7, whereby the plug and the wiring are formed at the same time.

BSTX:
[0016] First, as shown in FIG. 2A, wiring recesses are formed in a silicon oxide film 12 formed on a semiconductor substrate 11, and then underlying wirings 13 are buried in the recesses. Then, a low dielectric constant resin film 14 and a first photoresist film 15 with low sensitivity are formed in sequence on the silicon oxide film 12 and the underlying wirings 13. Then, a hole latent image 15a in the first photoresist film 15 is formed by exposing. Then, a **second** photoresist film 16 with high sensitivity is coated on the **first** resist film 15. A latent image 16a of a wiring is then formed by exposing the second photoresist film 16. A part of the wiring latent image 16a is formed to overlap with the hole latent image 15a. Then, as shown in FIG. 2B, the **first** photoresist film 15 and the **second** photoresist film 16 are developed successively, so that the wiring latent image 16a is removed to form a wiring

window 16b and also the hole latent image 15a is removed to form a hole window
15b. After this, the **first** photoresist film 15, the **second** photoresist film
16, and the low dielectric constant resin film 14 are etched sequentially from
the upper side, as shown in FIG. 2C. As a result, a vertical contact hole 17
and a wiring recess 18 are formed in the low dielectric constant resin film 14.
The copper (not shown) is buried in the vertical contact hole 17 and the wiring
recess 18 simultaneously. Such copper is used as the plug in the vertical
contact hole 17 and also used as the wiring in the wiring recess 18.

BSTX:
[0020] In addition, in the steps shown in FIGS. 2A to 2C, three different resin
materials of the low dielectric constant resin film 14, the **first** photoresist
film 15, and the **second** photoresist film 16 must be etched at the same etching
rate. However, respective etching rates of these resin materials are different
depending upon the width of the wiring recess 18 and the diameter of the
vertical contact hole 17. Therefore, if the wiring recesses each having a
different profile or width, or the vertical contact holes 17 each having a
different diameter are to be formed in the same layer, it is difficult to etch
these resin materials while controlling respective layers to coincide with
their designed dimensions.

BSTX:
[0022] According to an aspect of the present invention, after a **first**
insulating film, an organic insulating film, a **second** insulating film, and a
metal film are formed in sequence over a substrate, an opening having a wiring
pattern is formed in the metal film by the photolithography, then an opening

having a via pattern profile is formed in the **second** insulating film by the photolithography, then the organic insulating film is etched using the **second** insulating film as a mask, then the **first** insulating film and the **second** insulating film are etched simultaneously while using the metal film and the organic insulating film as a mask, and then the organic insulating film is etched while using the **second** insulating film as a mask. At this stage, a wiring recess is formed in the organic insulating film and the **second** insulating film, and a via-hole is formed in the **first** insulating film.

BSTX:
[0024] In addition, when the underlying organic insulating film is etched by using the second insulating film as a mask, the resist on the second insulating film can be removed simultaneously with the etching of the organic insulating film. Thereby, there is no need that the resist should be removed solely, and the underlying organic insulating film which is exposed is not badly affected at all in removing the resist. Accordingly, the wiring recess and the via can be formed with high precision by applying not only fluorocarbon **polymer** but also hydrocarbon resin as constituent material of the organic insulating film.

BSTX:
[0025] Furthermore, since the **first** insulating film, the organic insulating film, and the **second** insulating film are sequentially etched under the optimum condition, the via-hole or the wiring recess can be formed in these films with high precision.

BSTX:
[0026] According to another aspect of the present invention, after the **first**

insulating film, the organic insulating film, and the **second** insulating film
are formed in sequence, an opening having a via pattern profile is formed in
the **second** insulating film by the photolithography, then an opening having the
via pattern profile is formed in the organic insulating film through the
opening of the second insulating film, then an opening having a wiring pattern
profile is formed in the **second** insulating film by the photolithography and at
the same time an opening having the via pattern profile is formed by etching
the **first** insulating film using the organic insulating film as a mask, and then
an opening having the wiring pattern profile is formed by etching the organic
insulating film while using the **second** insulating film as a mask.

BSTX:
[0028] Moreover, after the opening having the wiring pattern profile is formed
in the second insulating film and then the opening having the via-hole profile
is formed in the underlying organic insulating film, these opening profiles are
transferred sequentially onto the insulating films positioned below them.
Therefore, the wiring recess and the via-hole can be formed in the **first**
insulating film, the **second** insulating film and the organic insulating film.
As a result, the **first** insulating film, the **second** insulating film, and the
organic insulating film can be etched individually under their optimum
conditions, so that the wiring recess and the via-hole can be formed with high
precision.

BSTX:
[0030] The underlying organic insulating film may be interposed between the
first insulating film and the **second** insulating film. The etching of the

underlying organic insulating film may be carried out simultaneously when the
overlying organic insulating film is etched.

BSTX:
[0031] According to still another aspect of the present invention, after the
first insulating film and the **second** insulating film have been formed in
sequence over the substrate, the opening having the via-hole pattern profile is
formed in the **first** insulating film and the **second** insulating film by using the
first photoresist, and then the opening having the wiring pattern profile is
formed by etching the **second** insulating film and the upper portion of the **first**
insulating film by using the **second** photoresist.

BSTX:
[0032] In this way, if the organic insulating material is adopted as the **first**
insulating film, both the step of removing the resist used to form the opening
and the step of forming the opening having the via pattern profile in the
organic insulating film while using the **second** insulating film as a mask can be
executed simultaneously by forming the opening having the via pattern profile
in the **second** insulating film. Therefore, the first insulating film formed of
the underlying organic insulating material is never etched into the unnecessary
size in removing the first resist, so that the precision of the opening in the
organic insulating film is never degraded.

DRTX:
[0039] FIG. 5 is a view relationships between a diameter of a contact via
formed by the **first embodiment and the second** embodiment and yield;

DRTX:
[0040] FIG. 6 is a view showing relationships between a distance between

wirings formed by the **first embodiment and the second** embodiment and a capacitance ratio of the wirings, while comparing with the conventional relationship;

DETX:
[0047] FIG. 3A shows the structure in which a **first** silicon oxide film (SiO.sub.2 film) 22, a **first** organic insulating film 23, a **second** silicon oxide film 24, and a photoresist film 25 are formed on a silicon substrate 21.

DETX:
[0048] The **first** silicon oxide film 22 and the **second** silicon oxide film 24 are formed by the plasma CVD method to have a thickness of 200 nm and a thickness of 100 nm respectively.

DETX:
[0051] Then, as shown in FIG. 3B, openings 24a each having a wiring pattern profile are formed by etching the second silicon oxide film 24 through the windows 25a of the photoresist film 25. The etching of the second silicon oxide film 24 is carried out by the plasma etching method using a CF.sub.4 gas, a CH.sub.2F.sub.2 gas, and an Ar gas. Since such etching gas belongs to a fluorocarbon group, the **second** silicon oxide film 24 is etched selectively to thus form the wiring openings 24a, nevertheless the **first** organic insulating film 23 under the **second** silicon oxide film 24 is seldom etched.

DETX:
[0052] Then, as shown in FIG. 3C, with the use of the plasma etching method, openings 23a for wiring pattern profiles are formed by removing the part of the **first** organic insulating film 23, which is exposed from the wiring openings 24a of the **second** silicon oxide film 24.

DETX:
[0054] A **first** wiring recess 26 consists of the opening 24a of the **second** silicon oxide film 24 and the opening 23a of the **first** organic insulating film 23, which are formed by the above patterning processes.

DETX:
[0056] The opening 23a of the **first** organic insulating film 23 and the opening 24a of the **second** silicon oxide film 24 are overlapped vertically with each other, and are used as the **first** wiring recess 26.

DETX:
[0057] Then, as shown in FIG. 3D, a **first barrier** metal film 27 made of TiN or TaN as a refractory metal is formed in the **first** wiring recess 26 and on the **second** silicon oxide film 24 by the sputtering to have a thickness of 50 nm. Then, a **first** copper (Cu) film 28 is similarly formed on the **first barrier** metal film 27 by the sputtering to have a thickness of 800 nm.

DETX:
[0059] Subsequently, as shown in FIG. 3E, the **first** Cu film 28 and the **first barrier** metal film 27 are polished by using the chemical mechanical polishing (CMP) method. Thus, the **first** Cu film 28 and the **first barrier** metal film 27 remain only in the **first** wiring recess 26, and they are employed as a **first** wiring 29.

DETX:
[0060] Then, as shown in FIG. 3F, a plurality of insulating film, metal film, etc., to be described in the following, are formed on the **first** wirings 29 and the **second** silicon oxide film 24.

DETX:

[0061] More particularly, a 50 nm thick silicon nitride film 30 and a 600 nm thick third silicon oxide film 31 are formed by the plasma CVD method on the **first** wirings 29 and the **second** silicon oxide film 24. Then, a second organic insulating film 32 of 400 nm thickness is formed by the spin coating on the third silicon oxide film 31. In this case, any one of above materials employed for the **first** organic insulating film 23 may be selected as the **second** organic insulating film 32. In turn, a fourth silicon oxide film 33 of 100 nm thickness is formed on the second organic insulating film 32 by the plasma CVD method. Then, an intermediate metal film 34 made of TiN is formed on the fourth silicon oxide film 33 by the sputtering to have a thickness of 100 nm. As the intermediate metal film 34, it is possible to use other refractory metal or refractory metal compound, e.g., tantalum (Ta) or tantalum nitride (TaN), in addition to TiN.

DETX:
[0071] Then, as shown in FIG. 3N, a **second barrier** metal film 39 made of TiN or TaN and having a thickness of 50 nm is formed by the sputtering along inner surfaces of the **second** wiring recess 37 and the contact via-hole 38 and an upper surface of the intermediate metal film 34. Then, a second copper film 40 is formed by the sputtering to have a thickness of 100 nm.

DETX:
[0082] In the **first** embodiment, the intermediate metal film 34 is formed on the fourth silicon oxide film 33, and then the opening 34a for the **second** wiring is formed in the intermediate metal film 34. In a second embodiment of the present invention, a method of forming the second wiring recess 37 and the contact via-hole without the intermediate metal film 34

will be explained
hereunder.

DETX:
[0089] **First, when the second** organic insulating film 32 is etched through a
wiring opening 33d of the fourth silicon oxide film 33, a wiring opening 32d is
formed in the position to contain the opening 32c. In this case, the plasma
anisotropic etching method using the oxygen containing gas is employed to etch
the second organic insulating film 32, so that the photoresist 45 can be etched
simultaneously and thus removed. The second wiring recess 37 is composed of
the wiring opening 33d of the fourth silicon oxide film 33 and the wiring
opening 32d of the second organic insulating film 32.

DETX:
[0091] After this, as shown in FIG. 4G, via the steps similar to those in the
first embodiment, a via 43 made of copper is buried in the contact via-hole 38
and also a **second** wiring 42 is buried in the **second** wiring recess 37.

DETX:
[0092] In the **second** embodiment, unlike the **first** embodiment, the photoresist
is employed instead of the metal film, as a mask to form the opening
corresponding to the contact via in the fourth silicon oxide film 33.

DETX:
[0095] By the way, when relationships between the diameter of contact via
formed by the above **first and second** embodiments and yield are examined
experimentally, the results shown in FIG. 5 are obtained.

DETX:
[0096] FIG. 5 shows the yield of the via plug which is obtained by measuring
the contact resistance of the via plug and then deciding

the via plug whose
contact resistance exceeds a theoretical value by more than 10% as the
defective. Such via plug connects the **first** layer wiring and the **second** layer
wiring in the double-layered wirings which are formed according to the **first**
embodiment and the second embodiment. The abscissa in FIG. 5 denotes the
diameter of the via contact. As indicated by this result, the high yield in
excess of 97 t can be achieved at any via diameter.

DETX:
[0097] Next, when the lateral wiring distance and the capacitance ratio in the
lateral direction are examined experimentally in the wirings which are formed
according to the **first embodiment and the second** embodiment respectively, the
results shown in FIG. 6 are obtained.

DETX:
[0098] FIG. 6 shows the wiring capacitance ratio which is obtained by measuring
the wiring capacitance in the same layer of the double-layered wirings, which
are formed according to the **first embodiment and the second** embodiment, and
then comparing it with the wiring capacitance generated when only the SiO.sub.2
film is employed in the prior art. The abscissa in FIG. 13 denotes the
distance between the wirings. As indicated by this result, the wiring
capacitance ratio can be reduced in the range from 60% to 65%. This ratio is
substantially equal to the ratio of the dielectric constant 4.3 of SiO.sub.2
and the dielectric constant 2.8 of the organic insulating film, which shows the
fact that the wirings have been formed satisfactorily.

DETX:
[0100] In the **first embodiment or the second** embodiment, another organic
insulating film may be formed between the silicon nitride

film 30 and the third
silicon oxide film 31.

DETX:
[0102] After the opening 50a is formed, a part of the **first** wiring is exposed
by etching the silicon nitride film 30 through the opening 50a and then the
conductive film is buried in the via-hole and the wiring recess to thus form
the **via and the second** wiring, like the **first embodiment and the second**
embodiment.

DETX:
[0105] In the **first embodiment and the second** embodiment, the insulating layer
into which the **second** copper wiring and the via (plug) are buried includes not
only the organic insulating film but also the silicon oxide film. In a fourth
embodiment, steps of forming a multilevel wiring structure in which the second
copper wiring and the via (plug) are buried in the organic insulating film will
be explained hereunder.

DETX:
[0108] In addition, a first organic insulating film 54 of low dielectric
constant is formed on the first silicon nitride film 53. For example, the
first organic insulating film 54 may be formed by coating the low dielectric
constant organic insulating material formed of the hydrocarbon group containing
the aromatic material on the first silicon nitride film 53 **via the spin** coating
to have a thickness of 300 nm, and then curing the organic insulating material
for 30 minutes via the thermal annealing at the temperature of 400.degree. C.
in the nitrogen (N.sub.2) atmosphere. As the low dielectric constant organic
insulating material formed of the hydrocarbon group containing the aromatic
material, for example, there is "SiLK" (product name)

manufactured by The Dow
Chemical Co. The dielectric constant of "SiLK" is about
2.7.

DETX:
[0109] Then, a **second** silicon oxide film 55 is formed on the **first** organic
insulating film 54 by the plasma CVD method to have a thickness of 100 nm.

DETX:
[0112] A **first** wiring recess 57 is composed of the opening 55a of the **second**
silicon oxide film 55 and the opening 54a of the **first** organic insulating film
54.

DETX:
[0113] Then, as shown in FIG. 8E, a **first barrier** metal film 58 is formed by
the sputtering in the inside of the **first** wiring recess 57 and on the upper
surface of the **second** silicon oxide film 55. The **first barrier** metal film 58
is formed of tantalum nitride (TaN) as a refractory metal and has a thickness
of 20 nm. Then, a **first** copper (Cu) film 59 is formed on the **first barrier**
metal film 58 by the sputtering to have a thickness of 800 nm.

DETX:
[0115] Subsequently, as shown in FIG. 8F, the **first** copper film 59 and the
first barrier metal film 58 are polished by using the chemical mechanical
polishing (CMP) method. Thus, the **first** copper film 59 and the **first barrier**
metal film 58 remain only in the **first** wiring recess 57, and they are employed
as a **first** wiring 60.

DETX:
[0116] Then, as shown in FIG. 8G, a plurality of insulating film, metal film,
etc., to be described in the following, are formed on the

first wiring 60 and
the second silicon oxide film 55.

DETX:
[0117] First, a second silicon nitride (Si.sub.3N.sub.4) film 61 of 50 nm
thickness is formed on the first wiring 60 and the second silicon oxide film 55
by the plasma CVD method. Then, a second organic insulating film 62 of about
100 nm thickness is formed on the second silicon nitride film 61. The second
organic insulating film 62 is formed by the same method as the first organic
insulating film 54 using the insulating material such as "SiLK".

DETX:
[0126] Next, as shown in FIG. 8M, the second Si.sub.3N.sub.4 film formed
directly below the contact hole 65 is removed by the plasma etching method
using C.sub.4F.sub.8 and O.sub.2, whereby a part of the first wiring 60 can be
exposed.

DETX:
[0127] Then, as shown in FIG. 8N, a TaN film 68 of 20 nm thickness is formed as
a barrier metal by the sputtering along the inner surfaces of the second wiring
recess 67 and the contact hole 65, and the upper surface of the third silicon
oxide film 63. Then, a copper seed film 69 of 150 nm thickness is formed on
the TaN film 68 by the sputtering.

CLTX:
1. A semiconductor device manufacturing method comprising the steps of:
forming a first insulating film, a first organic insulating film, a second
insulating film, and a metal film in sequence on a semiconductor substrate;
forming a first opening having a wiring pattern profile by etching the metal
film partially; forming a second opening having a via

pattern profile by
etching a portion of the **second** insulating film which overlaps with a part of
the **first opening**; forming a third opening having the via pattern profile in
the **first** organic insulating film by etching the **first** organic insulating film
through the **second opening** using the **second** insulating film as a mask; forming
a fourth opening having the wiring pattern profile in the **second** insulating
film by etching the **second** insulating film through the **first opening** of the
metal film, and simultaneously forming a fifth opening having the via pattern
profile by etching the **first** insulating film through the third **opening of the**
first organic insulating film, the fifth opening being applied as the via-hole;
forming a sixth opening having the wiring pattern profile in the **first** organic
insulating film by etching the **first** organic insulating film through the fourth
opening of the second insulating film, the sixth opening and the fourth opening
being applied to a wiring recess; forming a via in the via-hole and forming a
wiring in the wiring recess by burying a conductive material simultaneously
into the via-hole and the wiring recess; and removing the metal film.

CLTX:
3. A semiconductor device manufacturing method according to claim 1, further
comprising the step of: forming a **second** organic insulating film between the
first insulating film and the third insulating film; and forming an eighth
opening in the second organic insulating film by etching the **second** organic
insulating film through the fifth **opening of the first** insulating film at a
same time when the sixth opening is formed in the **first** organic insulating
film; wherein the eighth opening, the fifth opening and

the seventh opening
are applied as the via-hole.

CLTX:
5. A semiconductor device manufacturing method according to claim 1, wherein
the **first** insulating film and the **second** insulating film are formed of
inorganic insulating material.

CLTX:
8. A semiconductor device manufacturing method according to claim 1, wherein a
resist mask is employed in forming the **first opening** in the metal film, and the
resist mask is removed before the **second opening** is formed.

CLTX:
9. A semiconductor device manufacturing method according to claim 1, wherein a
resist mask is employed in forming the **second opening in the second** insulating
film, and the resist mask is etched at a same time when a part of the **first**
organic insulating film is etched to form the third opening.

CLTX:
10. A semiconductor device manufacturing method comprising the steps of:
forming a **first** insulating film, a **first** organic insulating film, and a **second**
insulating film in sequence on a semiconductor substrate; forming a **first**
opening having a via pattern profile by etching the **second** insulating film
partially; forming a **second opening having a via** pattern profile in the **first**
organic insulating film by etching the **first** organic insulating film through
the **first opening of the second** insulating film; forming a third opening
having a wiring pattern profile by etching a portion of the **second** insulating
film which contains the **first opening,** and simultaneously forming a fourth

opening in the first insulating film by etching the **first** insulating film below
the **second** insulating film through the **second opening of the first** organic
insulating film, the fourth opening being applied as the via-hole; forming a
fifth **opening in the first** organic insulating film by etching the **first** organic
insulating film through the third **opening of the second** insulating film, the
fifth opening and the third opening being applied to a wiring recess; and
forming a via in the via-hole and forming a wiring in the wiring recess by
burying a conductive material simultaneously into the via-hole and the wiring
recess.

CLTX:
12. A semiconductor device manufacturing method according to claim 1, further
comprising the step of: forming a **second** organic insulating film between the
first insulating film and the third insulating film; and forming a seventh
opening in the second organic insulating film by etching the **second** organic
insulating film through the fourth **opening of the first** insulating film
simultaneously when the fifth opening is formed in the **first** organic insulating
film; wherein the eighth opening, the fifth opening and the seventh opening
are applied as the via-hole.

CLTX:
14. A semiconductor device manufacturing method according to claim 10, wherein
the **first** insulating film and the **second** insulating film are formed of
inorganic insulating material.

CLTX:
16. A semiconductor device manufacturing method according to claim 10, wherein
the **first opening of the second** insulating film is formed

by etching the **second**
insulating film using resist as a mask, and the resist is removed
simultaneously when the **first** insulating film is etched to form the **second**
opening.

CLTX:
17. A semiconductor device manufacturing method comprising the steps of:
forming a **first** insulating film and a **second** insulating film in sequence on a
semiconductor substrate; forming **first** photoresist including a **first** window
having a via pattern profile on the **second** insulating film; forming a **first**
opening having the via pattern profile by etching the **second** insulating film
using the **first** photoresist as a mask; forming a **second opening having the via**
pattern profile by etching the **first** insulating film through the **first opening**;
forming second photoresist having a wiring pattern on the second insulating
film; forming a third opening having the wiring pattern by etching the second
insulating film using the second photoresist as a mask; forming a fourth
opening having the wiring pattern by etching an upper portion of the first
insulating film through the third opening; and forming a wiring in the third
opening and the fourth opening and forming a via in the second opening by
burying a conductive material into the second opening, the third opening, and
the fourth opening.

CLTX:
18. A semiconductor device manufacturing method according to claim 17, wherein
the **first** photoresist is removed by using a hydroxylamine solvent after the
second opening has been formed.

CLTX:

20. A semiconductor device manufacturing method according to claim 17, wherein
the **first** insulating film is formed of hydrocarbon insulating material, and the
second insulating film is formed of silicon containing insulating material.

CLTX:
22. A semiconductor device manufacturing method according to claim 20, wherein
the silicon containing insulating material is formed of silicon oxide, silicon
nitride, silicon oxide nitride, or **silicon carbide**.

CLTX:
23. A semiconductor device manufacturing method according to claim 20, wherein
the **second opening** is formed by etching the **first** insulating film
simultaneously when the **first** photoresist is etched.

CLTX:
24. A semiconductor device manufacturing method according to claim 20, wherein
the fourth opening is formed by etching the **first** insulating film
simultaneously when the **second** photoresist is etched.